Predictive Gate Drive™ Frequently Asked Questions

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ABSTRACT

The proprietary Predictive Gate Drive™ technology from Texas Instuments maximizes efficiencies of today's high frequency, low output voltage, synchronous buck converters. To gain a better understanding of this innovative new control technique, this list of frequently asked questions (FAQs) addresses the Predictive Gate Drive™ technique.

Contents

1 Predictive Gate Drive General FAQs

1.1 What is Predictive Gate Drive™ technology?

Predictive Gate Drive™ technology is a digital control technique that virtually eliminates body-diode conduction while also minimizing reverse recovery losses in synchronous rectifiers. This can result in significant synchronous rectifier switching efficiency improvements.

1.2 How is body-diode conduction measured?

Switching waveforms in a typical synchronous buck application are shown in Figure 1 and Figure 2.

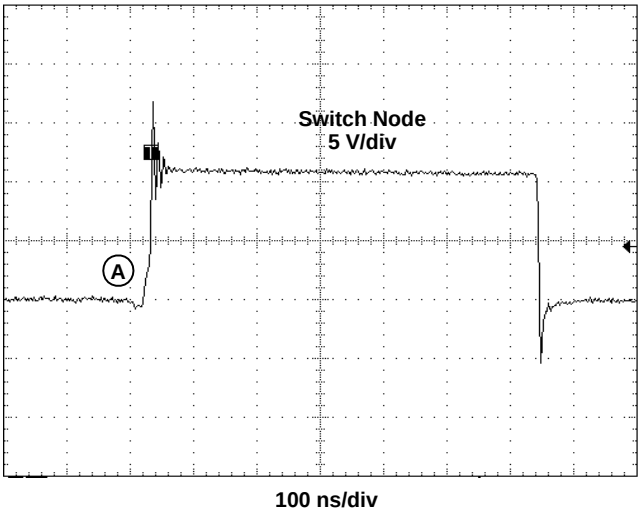

Figure 1. Switch-Node Voltage

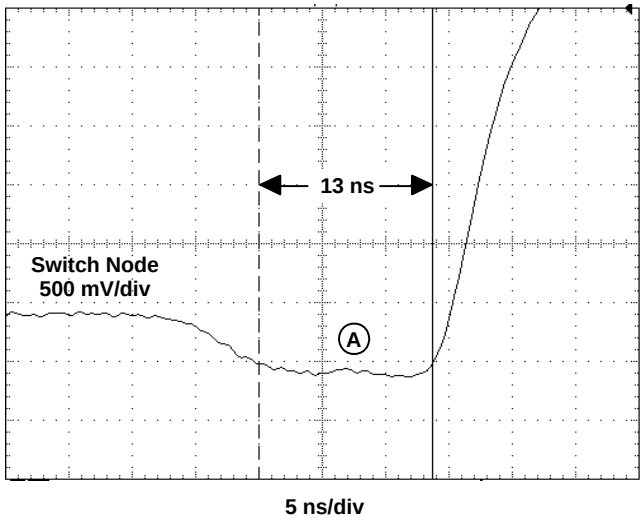

Figure 2. Switch-Node Voltage (Close-Up) of Point A

Figure 1 shows the drain-to-source voltage of the synchronous MOSFET in a 12-V synchronous buck application. This node, commonly referred to as the switch-node, is the point where the upper and lower MOSFET's connect to the output inductor. Body-diode conduction of the synchronous switch can be measured as the small dip labeled point A in Figure 1 and Figure 2. Similarly, some body-diode conduction exists at the falling edge of the switch-node as well. Point A, shown in Figures 1 and 2, is the time interval where neither the upper or lower MOSFET is conducting. During this brief time interval, the load current remains constant by flowing through the body-diode of the synchronous rectifier. A body-diode conduction time of 13 ns can be seen by zooming in on point A in a close up view as shown in Figure 2. For a synchronous buck converter not using Predictive Gate Drive™ technology, this time can be as long as 100 ns. Allowing the output current to flow through the body-diode of the synchronous rectifier has a degrading effect on overall efficiency. Predictive Gate Drive™ technology maximizes efficiency by reducing the delay time between turn-off of the high-side MOSFET and turn-on of the low-side MOSFET, in turn eliminating body-diode conduction time. Minimizing this delay time to near zero keeps the load current flowing where it belongs, through the conducting MOSFET switches.

1.3 How does Predictive Gate Drive™ eliminate body-diode conduction in a synchronous rectifier?

For the synchronous buck stage shown in Figure 3, Predictive Gate Drive™ starts by sensing the voltage at the switch-node (labeled point A), SWS, along with the gate voltage, G2S, of the synchronous rectifier.

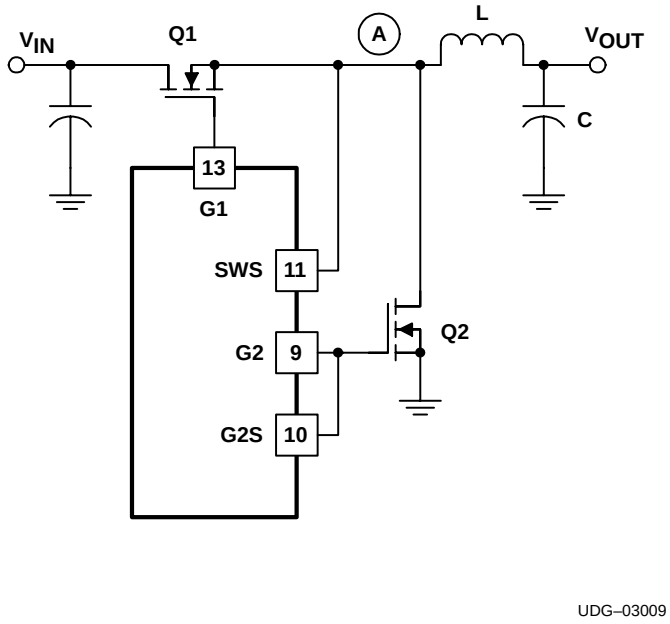

Figure 3. Sensing Q2 for Body-Diode Conduction

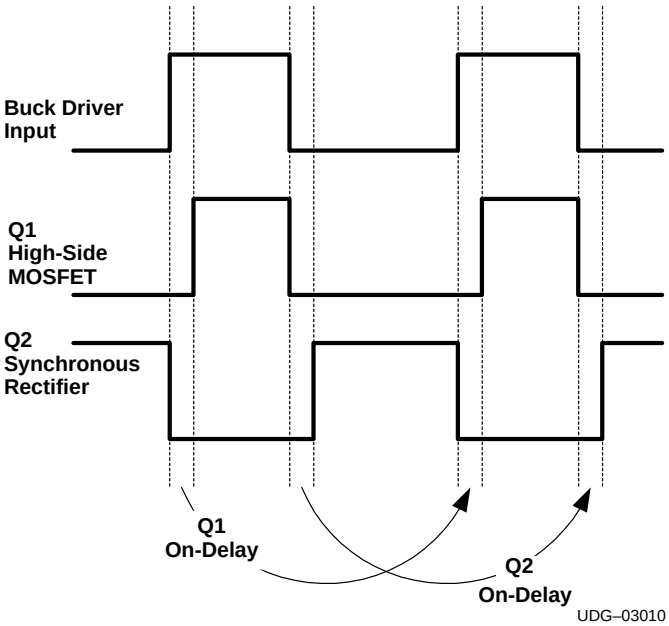

Figure 4. Predictive Timing

The smaller the delay time between Q2 turn-off and Q1 turn-on (as well as Q1 turn-off and Q2 turn-off), the less time that the body-diode of Q2 conducts. Ideally, if the delay time were zero, there theoretically would be zero body-diode conduction. Rather than sense the switch-node voltage for body-diode conduction and then adjust the delay time accordingly, Predictive Gate Drive™ uses information from the current switching cycle to *predict* the minimum delay time for the next cycle. This predictive concept is illustrated in Figure 4.

Predictive Gate Drive™ works on the premise that the delay time required for the next switching cycle is close to what was required for the previous cycle. When this assumption does not hold true, as in the case during a sudden line or load transient, Predictive Gate Drive™ operation requires some time to adjust to the changing operating conditions. During the time Predictive Gate Drive™ is recalibrating, there may be a very brief period of body-diode conduction in Q2, but this does not affect steady state efficiency or performance.

During the time that the PWM input signal transitions from high to low, a NOR gate senses the drain-to-source and gate-to-source voltage of Q2. If the NOR gate output is HIGH, as shown in Figure 5a, the delay is reduced by one bit of a 16-bit buffer delay line. In this example, each delay bit in the delay line represents a shift of approximately 4 ns. The delay is reduced by 4-ns intervals every switch cycle until the output of the NOR gate is low, as shown in Figure 5b. When the NOR gate output is low, the delay advances forward one delay unit on the next switching cycle. The process of continually shifting the delay forward and backward each cycle is known as *dithering*. When Predictive Gate Drive™ is optimal, dithering should occur within an 8-ns (2 delay bits) window.

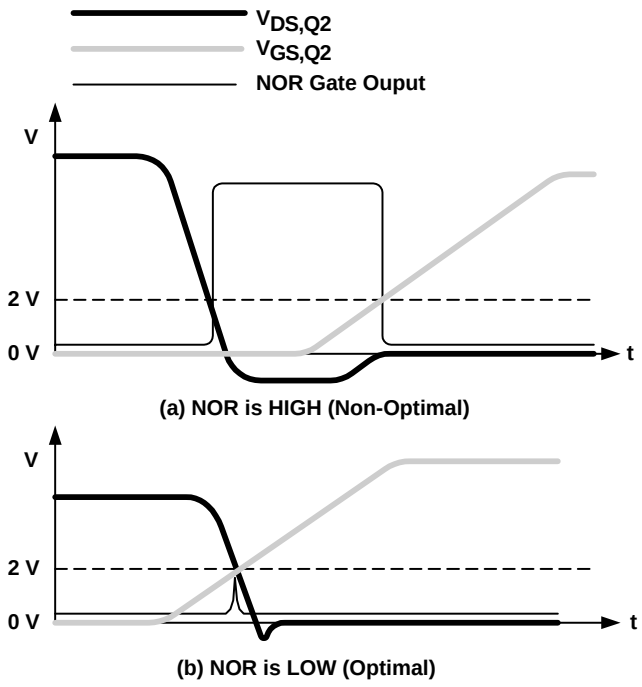

Figure 5. NOR Delays

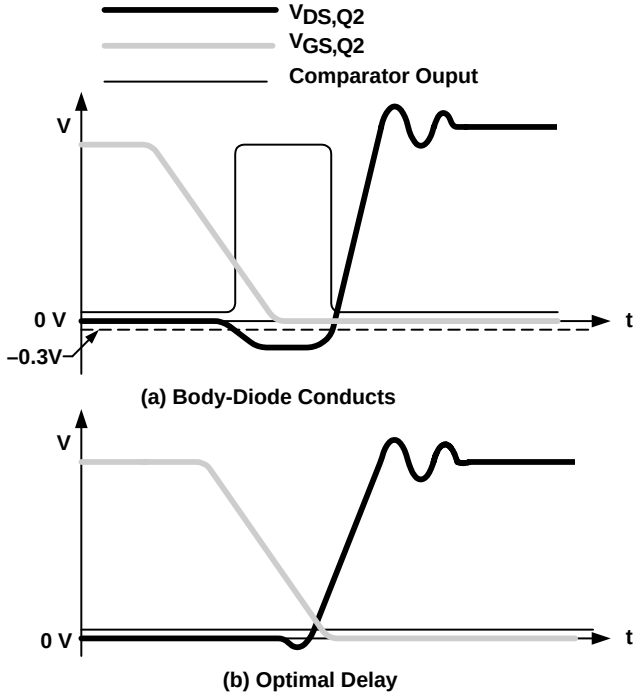

Figure 6. NOR Delays

Conversely, during the time the PWM input signal transitions from low to high, a comparator senses the drain-to-source and gate-to-source voltage of Q2. If body-diode conduction in Q2 is detected, the comparator output is HIGH, as shown in Figure 6a, and the delay time is once again reduced by one delay bit. Once enough delay segments have been introduced, such that the comparator output remains LOW, body-diode conduction in Q2 is now virtually zero, as shown in Figure 6b. From the optimal delay positioning of Figure 6b, the delay time increases by one delay bit on the next successive switch cycle. Dithering within 8-ns of this optimal delay then becomes apparent.

1.4 Does Predictive Gate Drive™ eliminate switching loss?

No. Predictive Gate Drive™ technology does not eliminate switching loss. Predictive Gate Drive™ minimizes body-diode conduction and reverse recovery losses that are typically a significant amount of the total device losses in a synchronous rectifier.

1.5 Does Predictive Gate Drive™ offer any benefit to the high-side MOSFET?

In addition to minimizing body-diode and reverse recovery losses in the synchronous rectifier, Predictive Gate Drive™ reduces power dissipation on the main (forward) MOSFET as well, although the savings is not as significant as that in the synchronous rectifier MOSFET.

The reason for this is that during reverse recovery the body diode is still forward biased, thus the reverse recovery current goes through the forward MOSFET while the drain-source voltage is still high, causing additional switching losses. During this transition, the switching losses in the high-side MOSFET are defined by the drain-to-source voltage and current as $V_{DS}=V_{IN}$ and $I_{DS}=I_{LOAD}+I_{RR}$, without Predictive Gate Drive™. When this technology is used, these same loss parameters are now defined by $V_{DS}=V_{IN}$ and $I_{DS}=I_{LOAD}$. The reduction in drain-to-source current explains the power savings in the high-side MOSFET. This can further be supported by comparing the thermal image shown in Figure 13, with Predictive Gate Drive™, to the image of Figure 14, without it.

1.6 Since Predictive Gate Drive™ utilizes a dithering or *hunting* technique to hone in on the optimal delay time, what impact does this have on EMI?

While there is some dithering associated with the Predictive Gate Drive™ control technique, this is expected and is not the same as gate-drive jitter commonly caused by high frequency noise. Unlike coupled noise that is random, high in di/dt content and varies with line and load, Predictive Gate Drive™ dithering is controlled with zero additional di/dt content and occurs within an 8-ns window area. In addition, since Predictive Gate Drive™ virtually eliminates body-diode conduction and reverse recovery, the high-frequency ringing commonly observed on the switch-node voltage of a synchronous buck is greatly reduced. Since switch-node ringing is a primary cause of radiated emissions, using the Predictive Gate Drive™ technology along with good PCB layout practices can significantly reduce EMI for a synchronous buck or multi-phase converter.

1.7 How does Predictive Gate Drive™ ensure that cross-conduction of the upper and lower switches does not occur?

Part of the Predictive Gate Drive™ control includes an internal delay line and comparator used to detect when the body-diode of the synchronous rectifier is conducting. Once this comparator detects body-diode conduction, the Predictive Gate Drive™ delay is adjusted to advance the delay time by one bit on the delay line. Because the comparator is slew-rate limited by the amount of time it takes to respond to a differential input voltage, it does not respond during the next cycle when body-diode conduction is now minimal. Since the delay time per element (typically 4 ns) of the delay line is less than the minimum detectable pulse width of the comparator, cross-conduction is completely avoided.

2 Competing Technologies

2.1 Do second sources offer similar synchronous rectification control techniques?

Predictive Gate Drive™ technology is unique and solely developed by Texas Instruments. A similar but different competing technology known as *adaptive delay* technology (also recognized as overlapping drive protection, adaptive shoot-through protection, anti-cross conduction) is also available from various manufacturers. Notable performance differences between Predictive Gate Drive™ and adaptive delay are shown below. The upper waveforms are complementary gate drives, while the lower waveform is the switch-node voltage. Notice the minimal body-diode conduction time shown in Figure 8 using Predictive Gate Drive™ versus the longer body-diode conduction interval associated with the adaptive delay control waveforms shown in Figure 7. Secondly, notice the reduced amount of ringing shown at the switch-node voltage in Figure 8.

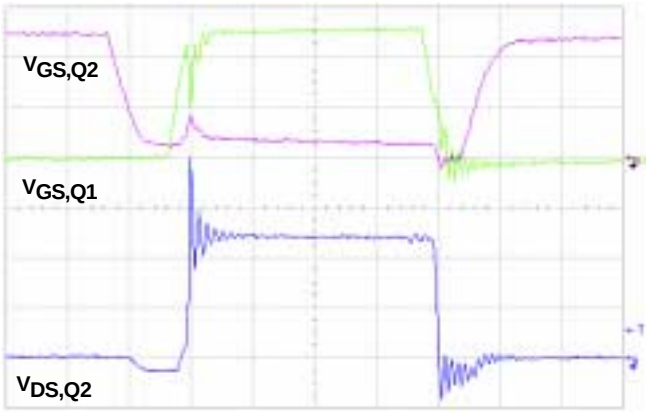

Figure 7. Adaptive Delay Control

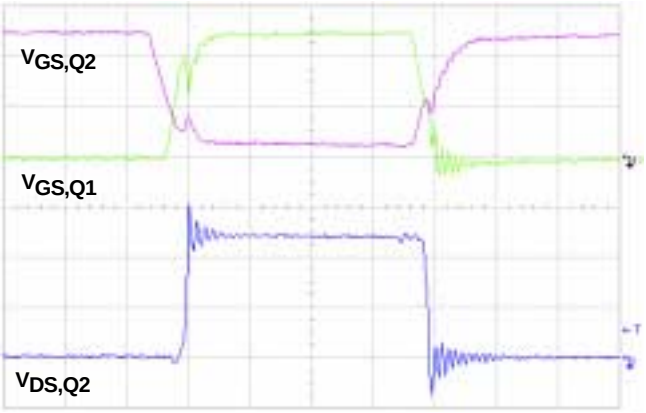

Figure 8. Predictive Gate Drive™ Techology

2.2 What is the difference between Predictive Gate Drive™ and Adaptive Delay Control?

Both of these control techniques aim to achieve the same thing, reducing the amount of delay time between turn-off of the main switch and turn-on of the synchronous switch in a synchronous buck regulator. Reduced delay time translates to minimizing body-diode conduction and reverse recovery time, which increases overall efficiency. The adaptive technique uses current state information from the power stage to control the turn-on of the two gate drivers. By the time the information is detected and processed, some finite dead time is still inevitable. The predictive technique is different from the adaptive technique in that it uses information from the previous switching cycle to set up the dead time for the current cycle. This information is processed in a way that allows the synchronous switch to begin to turn-on while the main switch is not yet fully turned off, yet cross-conduction is completely avoided. The result is that with Predictive Gate Drive™ technology, the dead time between the two switches is nearly zero, resulting in virtually no body-diode conduction.

3 Efficiency Improvements

3.1 How much overall efficiency improvement can be expected from Predictive Gate Drive™ technology?

The exact amount of efficiency gain using Predictive Gate Drive™ is highly dependant upon switching frequency and output voltage. As switching frequency is increased and output voltage is decreased, the efficiency gain of Predictive Gate Drive™ over adaptive delay increases. A 5 V-to-0.9 V converter running at 500 KHz using Predictive Gate Drive™ technology can realize an efficiency gain of nearly 4% over adaptive delay operating under similar conditions, as shown in Figure 9.

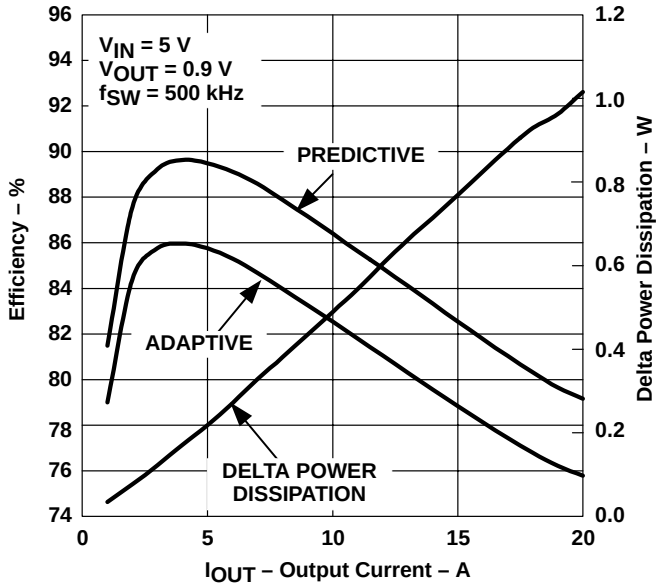

Figure 9. Predictive Gate Drive vs. Adaptive Delay Efficiency Improvement

3.2 What are the thermal efficiency improvements of Predictive Gate Drive™ versus Adaptive Delay control?

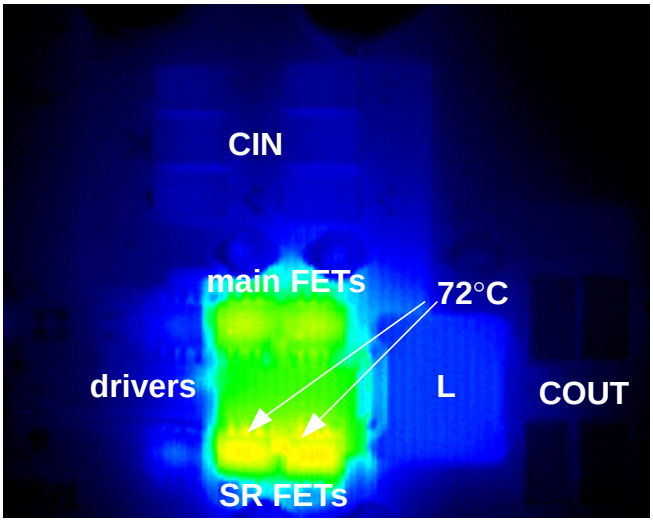

Figure 11. Predictive Gate Drive™

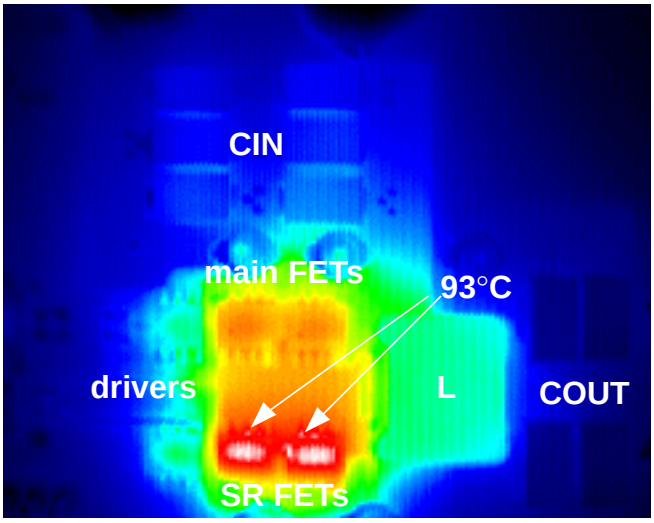

Figure 12. Adaptive Delay Control

White = 93°C, Yellow = 72°C, both images are scaled to the same unit measures. Approximately 21°C delta temperature rise in SR MOSFETs.

Both images shown in Figure 11 and Figure 12 were taken from identical synchronous buck power stages, operating at 500 KHz, from a 5-V input, with a 0.9-V output and a 20-A load. The converter also uses two Hitachi LF PAK MOSFET's in parallel for both the main MOSFETs and synchronous rectifiers.

Comparing the Predictive Gate Drive™ control to the adaptive delay control, the power stage using Predictive Gate Drive™ operates approximately 21°C cooler than the same power stage controlled by adaptive delay. As expected, the highest thermal benefit is recognized in the synchronous rectifiers controlled by Predictive Gate Drive™. To the power supply designer, this increase in thermal efficiency translates to lower junction temperatures resulting in increased component reliability, lower failure rates and higher mean time between failure (MTBF). For both power stages operating at similar temperatures, the thermal efficiency gains of a converter using Predictive Gate Drive™ can also be realized in the form of higher output current capability and/or higher operating frequency meaning smaller power stage components

4 References

1. Power Supply Design Seminar SEM-1400 Topic 2: *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments Literature No. SLUP169.
2. Power Supply Design Seminar SEM-1400 Topic 7: *Implication of Synchronous Rectifiers in Isolated, Single-Ended, Forward Converters*, by Christopher Bridge, Texas Instruments Literature No. SLUP175.
3. *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002.
4. *Predictive Gate Drive™ Boost Synchronous DC/DC Power Converter Efficiency*, by Steve Mappus, Texas Instruments Literature No. SLUA281.

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